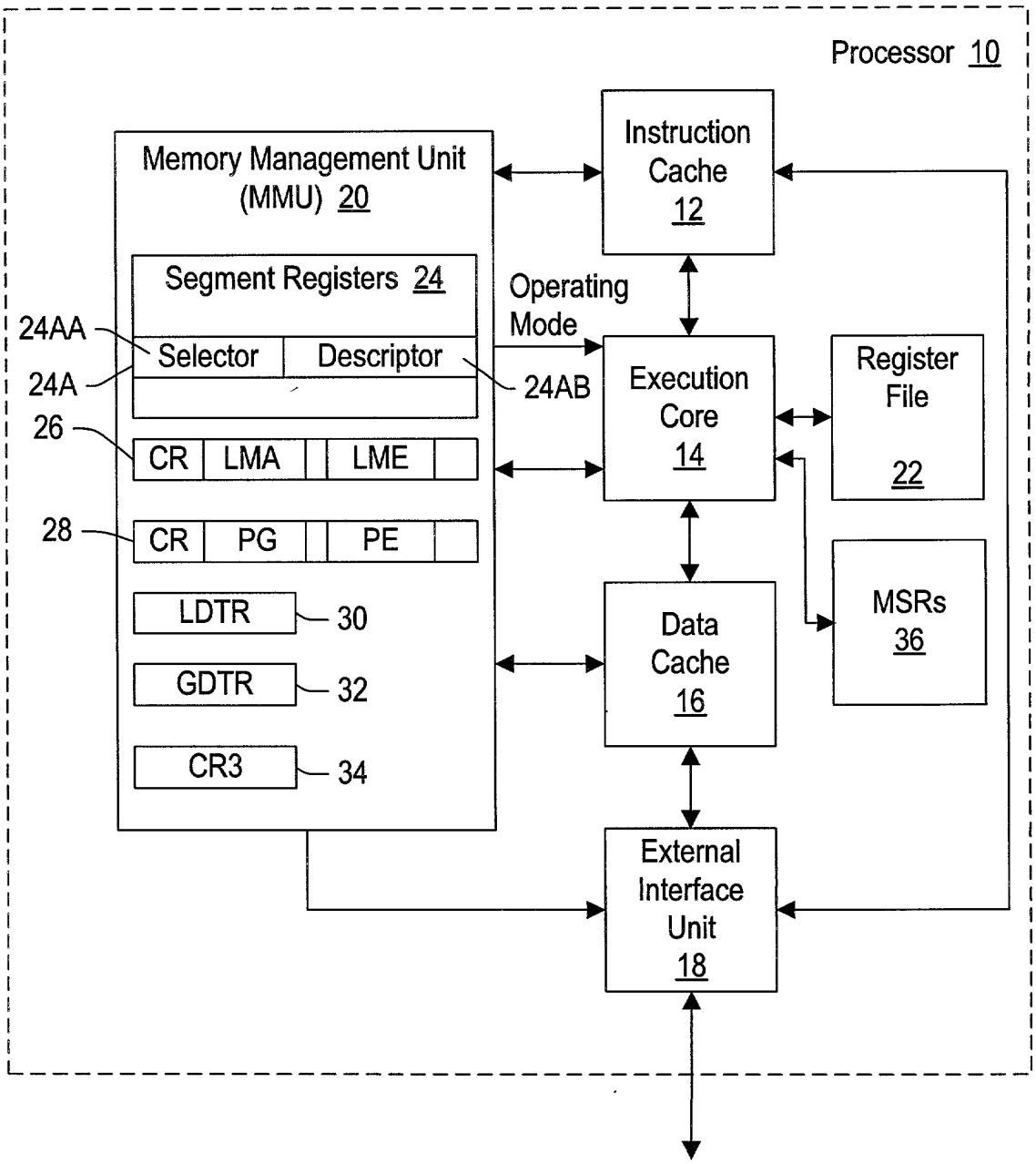

Processor 10
Memory Management Unit (MMU) 20
Segment Registers 24
24AA
Selector
Descriptor
24A
24AB
26
CR
LMA
LME
28
CR
PG
PE
LDTR
30
GDTR
32
CR3
34
Operating Mode
Instruction Cache 12
Execution Core 14
Register File 22
MSRs 36
Data Cache 16
External Interface Unit 18

Fig. 1

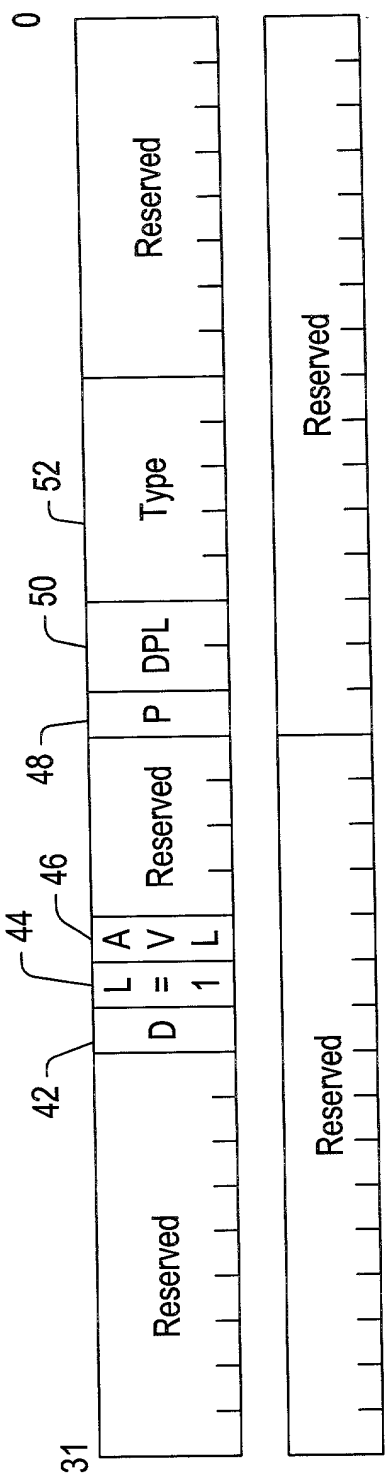

0
Reserved
Type
DPL
P
Reserved
A V L
L = 1
D
Reserved
31
42
44
46
48
50
52
Reserved
40

Fig. 2

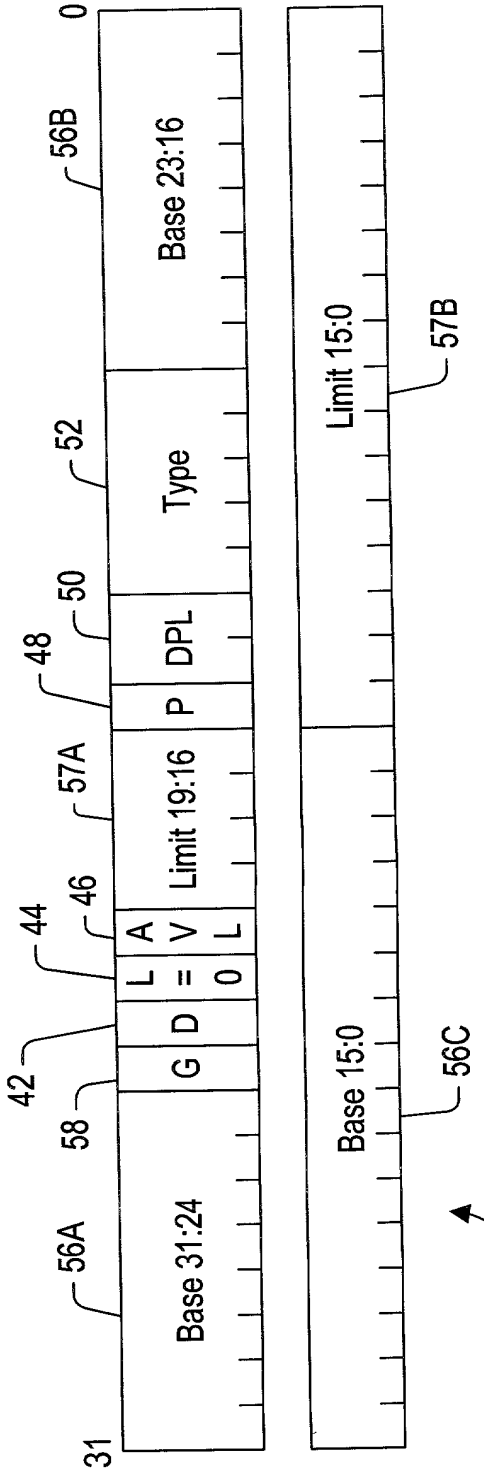

0
56B
Base 23:16
Type
DPL
P
Limit 19:16
A V L
L = 0
D
G
Base 31:24
Limit 15:0
Base 15:0
31
42
44
46
48
50
52
57A
57B
56A
56C
58
54

Fig. 3

LMA	CS L Bit	CS D Bit	Operating Mode
0	x	0	16 Bit Mode
0	x	1	32 Bit Mode
1	0	0	16 Bit Compatibility Mode
1	0	1	32 Bit Compatibility Mode
1	1	0	32/64 Mode
1	1	1	Reserved

70

Fig. 4

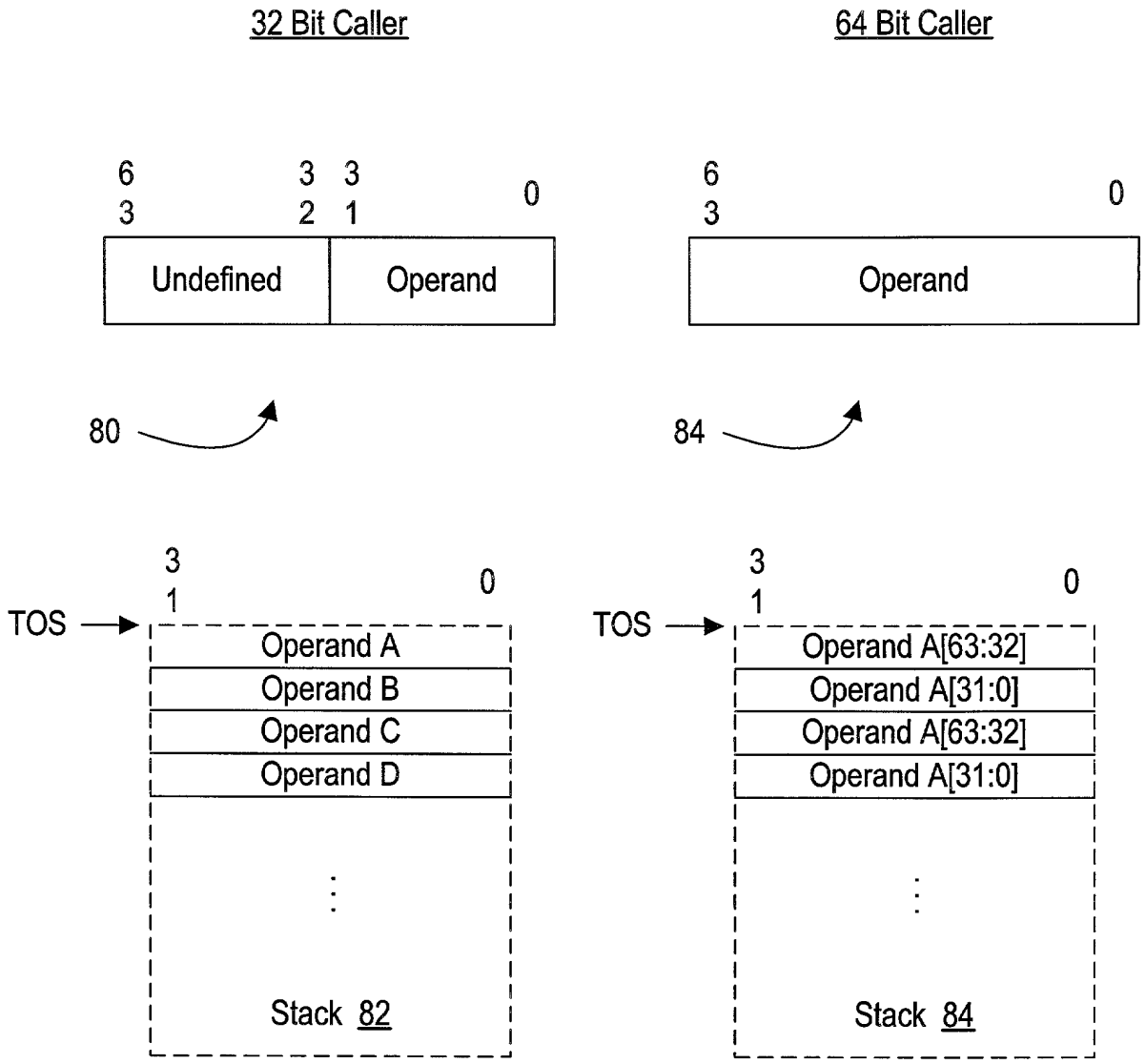

32 Bit Caller
64 Bit Caller
6 3
3 2
3 1
0
Undefined
Operand
Operand
80
84
TOS
3 1
0
Operand A
Operand B
Operand C
Operand D
Operand A[63:32]
Operand A[31:0]
Operand A[63:32]
Operand A[31:0]
Stack 82
Stack 84

Fig. 5

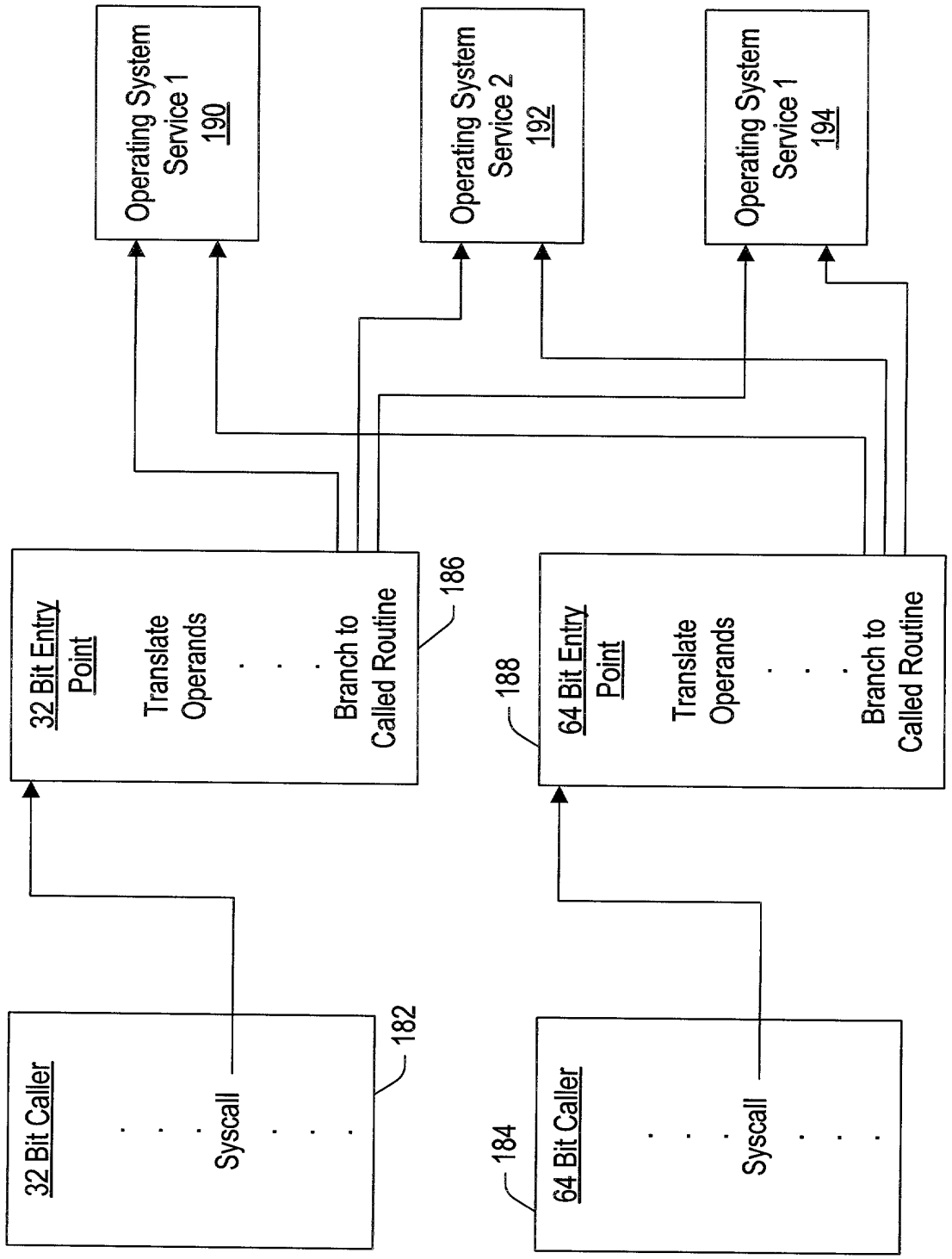

Operating System Service 1 190
Operating System Service 2 192
Operating System Service 1 194
32 Bit Entry Point
Translate Operands
Branch to Called Routine
186
64 Bit Entry Point
Translate Operands
Branch to Called Routine
188
32 Bit Caller
Syscall
182
64 Bit Caller
Syscall
184

Fig. 5A

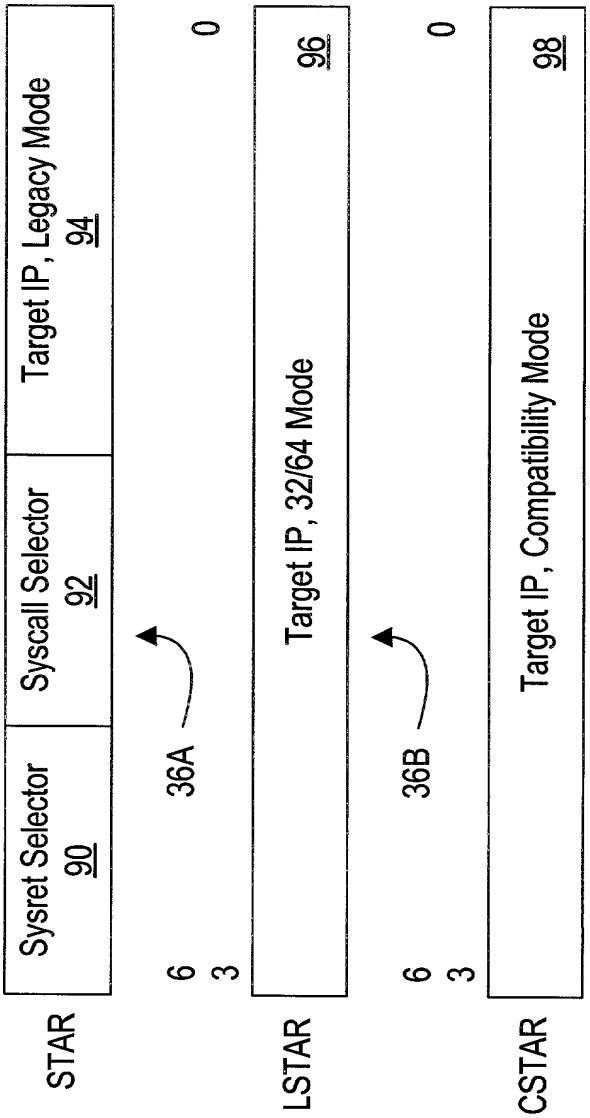

STAR
6 4 4 3 3 0
3 8 7 2 1
Sysret Selector 90
Syscall Selector 92
Target IP, Legacy Mode 94
36A
LSTAR
6 0
3
Target IP, 32/64 Mode 96
36B
CSTAR
6 0
3
Target IP, Compatibility Mode 98
36C

Fig. 6

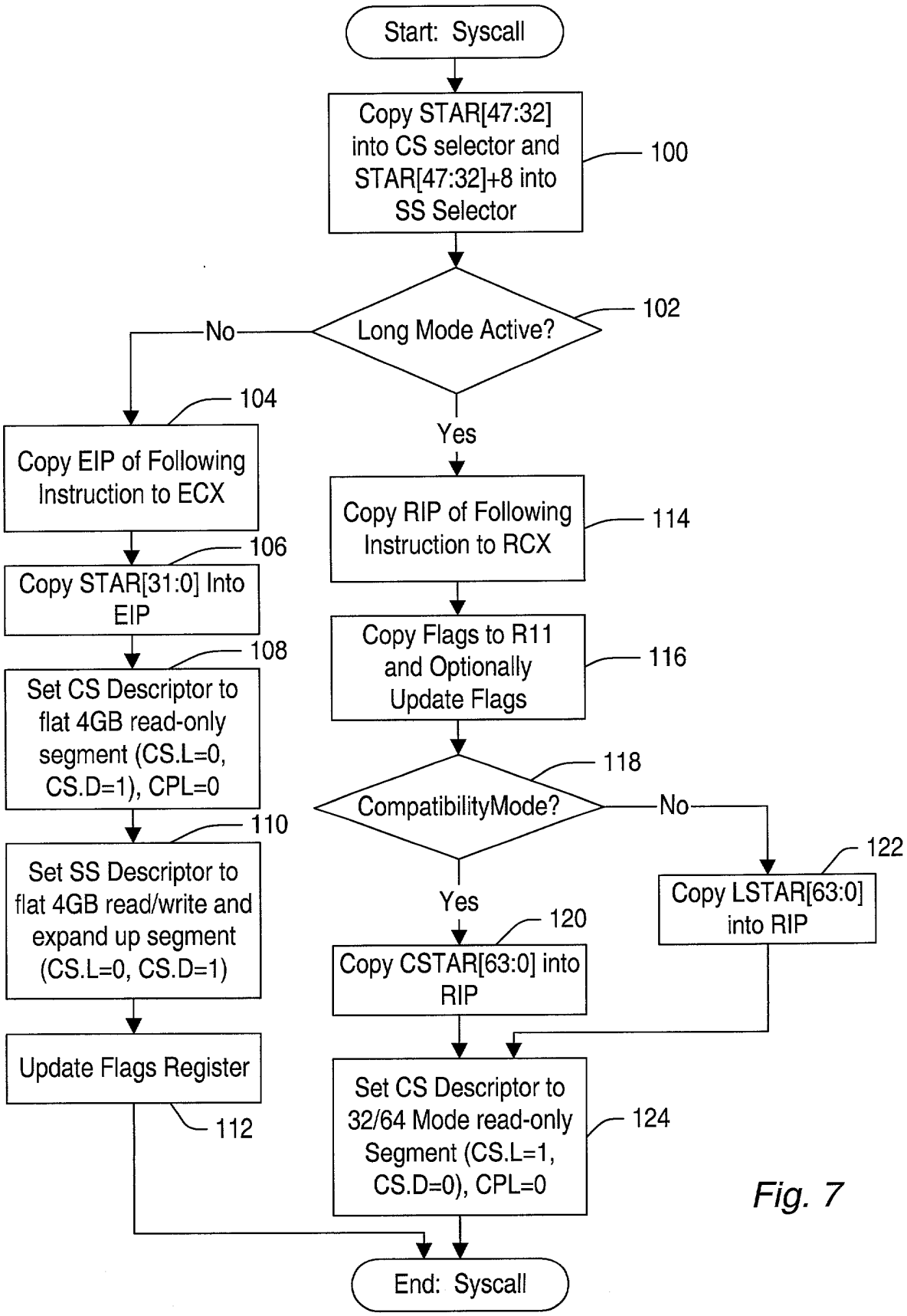

Start: Syscall
Copy STAR[47:32] into CS selector and STAR[47:32]+8 into SS Selector
100
Long Mode Active?
102
No
Yes
104
Copy EIP of Following Instruction to ECX
106
Copy STAR[31:0] Into EIP
108
Set CS Descriptor to flat 4GB read-only segment (CS.L=0, CS.D=1), CPL=0
110
Set SS Descriptor to flat 4GB read/write and expand up segment (CS.L=0, CS.D=1)
Update Flags Register
112
Copy RIP of Following Instruction to RCX
114
Copy Flags to R11 and Optionally Update Flags
116
CompatibilityMode?
118
No
Yes
120
Copy CSTAR[63:0] into RIP
122
Copy LSTAR[63:0] into RIP
Set CS Descriptor to 32/64 Mode read-only Segment (CS.L=1, CS.D=0), CPL=0
124
End: Syscall

Fig. 7

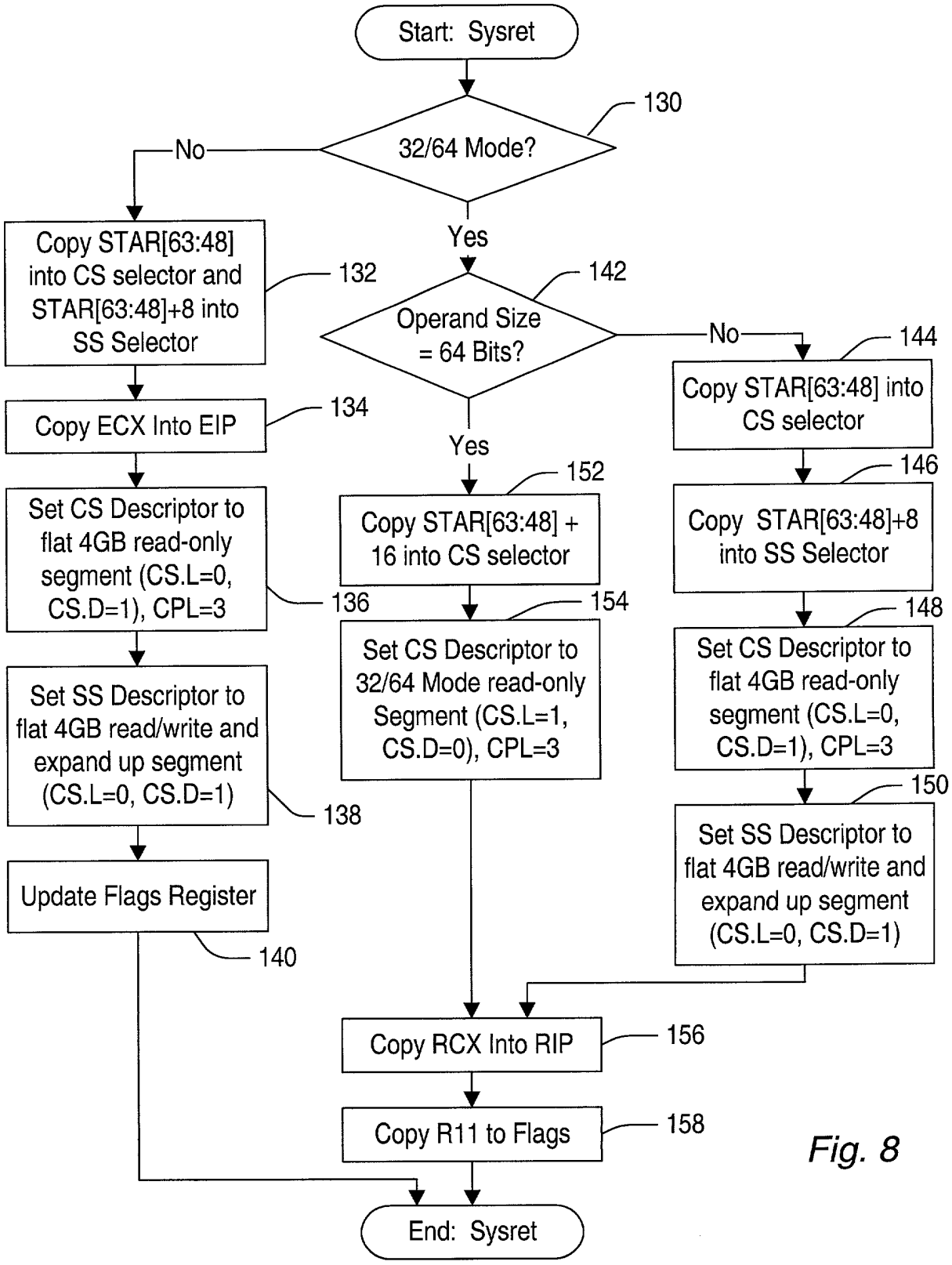
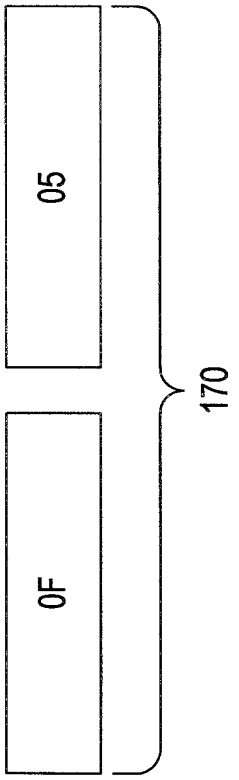

Start: Sysret
32/64 Mode?
130
No
Yes
Copy STAR[63:48] into CS selector and STAR[63:48]+8 into SS Selector
132
Operand Size = 64 Bits?
142
No
Yes
144
Copy STAR[63:48] into CS selector
Copy ECX Into EIP
134
Set CS Descriptor to flat 4GB read-only segment (CS.L=0, CS.D=1), CPL=3
136
Copy STAR[63:48] + 16 into CS selector
152
Copy STAR[63:48]+8 into SS Selector
146
Set CS Descriptor to 32/64 Mode read-only Segment (CS.L=1, CS.D=0), CPL=3
154
Set CS Descriptor to flat 4GB read-only segment (CS.L=0, CS.D=1), CPL=3
148
Set SS Descriptor to flat 4GB read/write and expand up segment (CS.L=0, CS.D=1)
138
Set SS Descriptor to flat 4GB read/write and expand up segment (CS.L=0, CS.D=1)
150
Update Flags Register
140
Copy RCX Into RIP
156
Copy R11 to Flags
158
End: Sysret

Fig. 8



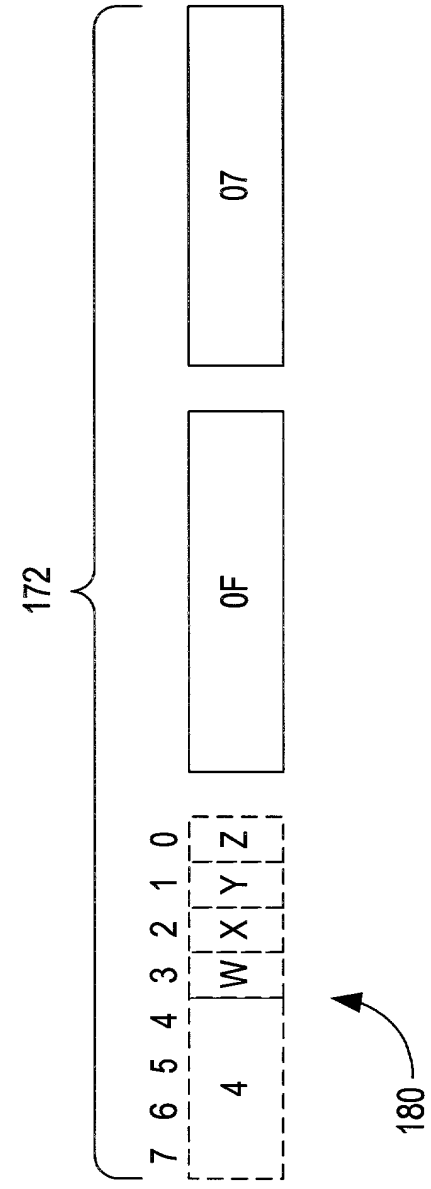


Fig. 9

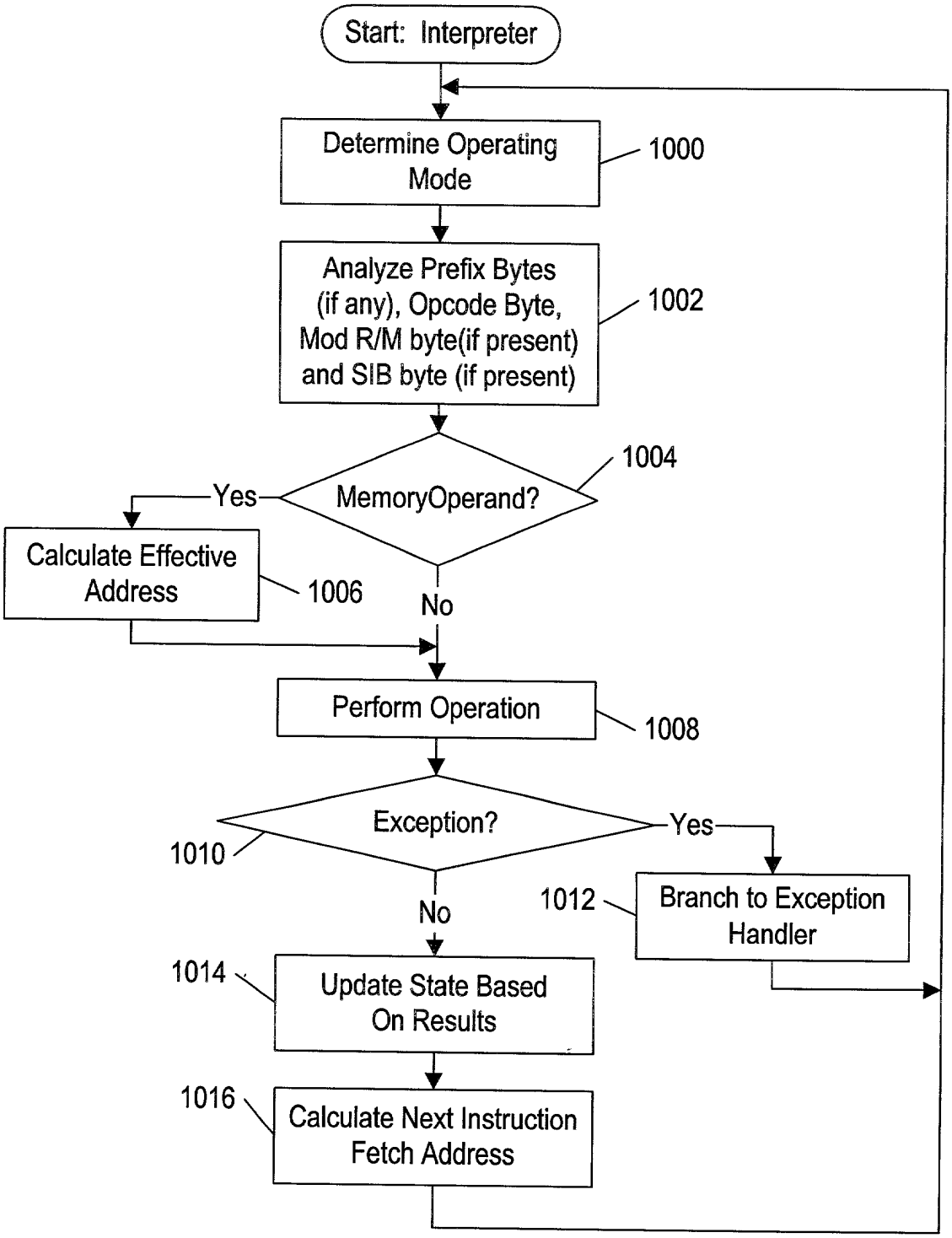

Start: Interpreter
Determine Operating Mode
1000
Analyze Prefix Bytes (if any), Opcode Byte, Mod R/M byte(if present) and SIB byte (if present)
1002
MemoryOperand?
1004
Yes
No
Calculate Effective Address
1006
Perform Operation
1008
Exception?
1010
Yes
No
Branch to Exception Handler
1012
Update State Based On Results
1014
Calculate Next Instruction Fetch Address
1016

Fig. 10

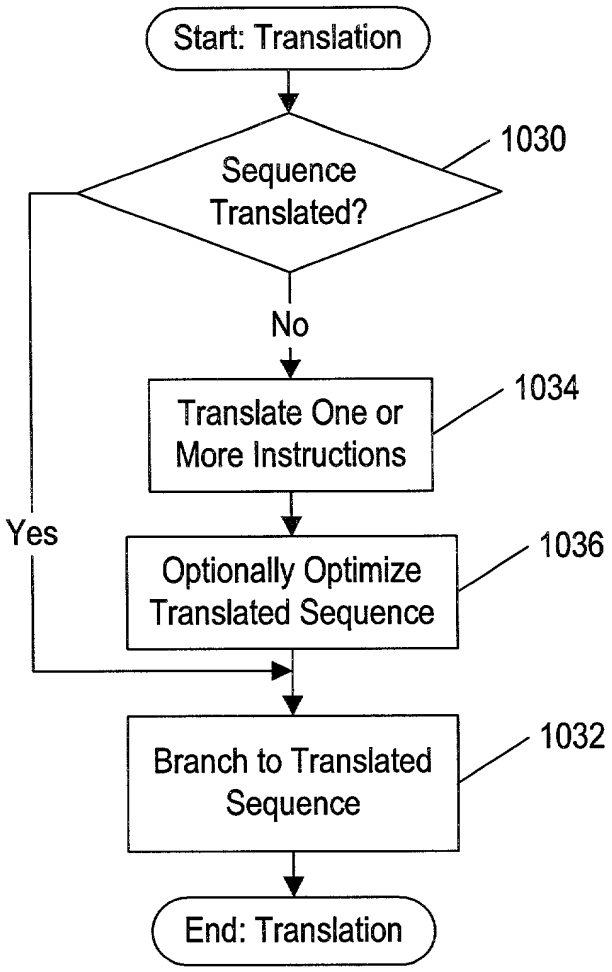

Start: Translation
Sequence Translated?
1030
No
Translate One or More Instructions
1034
Yes
Optionally Optimize Translated Sequence
1036
Branch to Translated Sequence
1032
End: Translation

Fig. 11

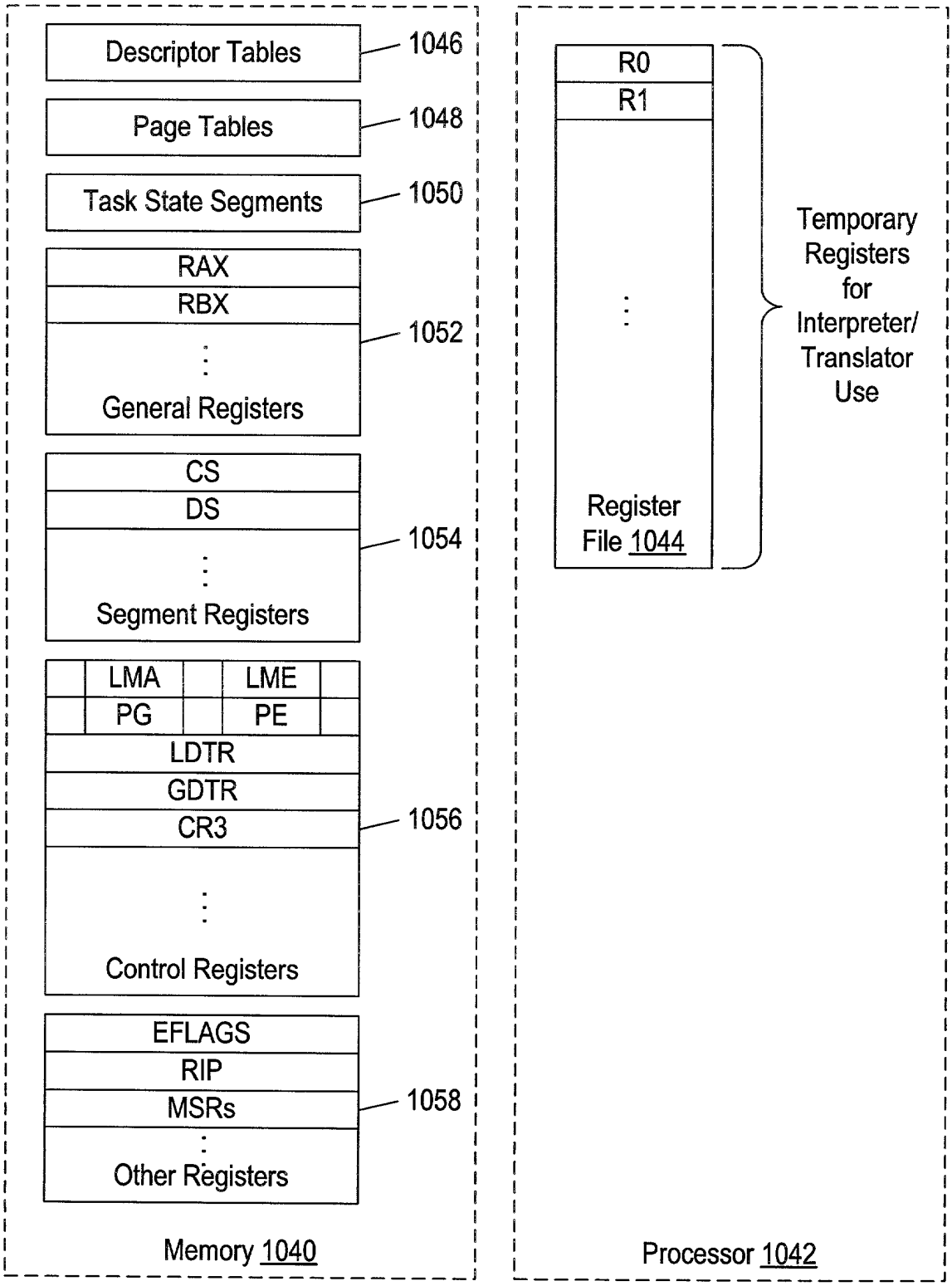

Descriptor Tables
1046
Page Tables
1048
Task State Segments
1050
RAX
RBX
General Registers
1052
CS
DS
Segment Registers
1054
LMA
LME
PG
PE
LDTR
GDTR
CR3
Control Registers
1056
EFLAGS
RIP
MSRs
Other Registers
1058
Memory 1040
R0
R1
Register File 1044
Temporary Registers for Interpreter/ Translator Use
Processor 1042

Fig. 12

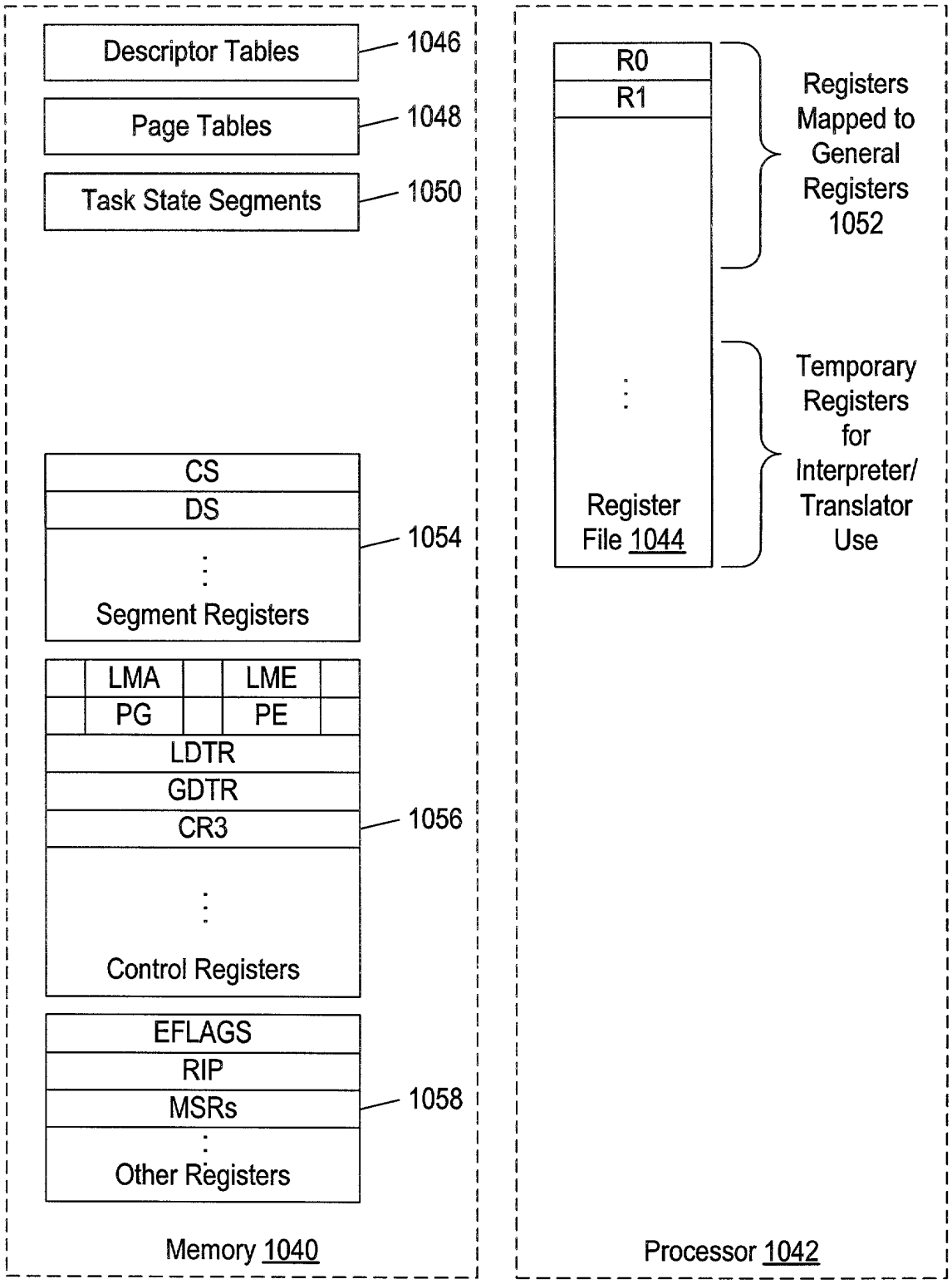

Descriptor Tables
1046
Page Tables
1048
Task State Segments
1050
CS
DS
Segment Registers
1054
LMA
LME
PG
PE
LDTR
GDTR
CR3
1056
Control Registers
EFLAGS
RIP
MSRs
1058
Other Registers
Memory 1040
R0
R1
Register File 1044
Registers Mapped to General Registers 1052
Temporary Registers for Interpreter/ Translator Use
Processor 1042

Fig. 13

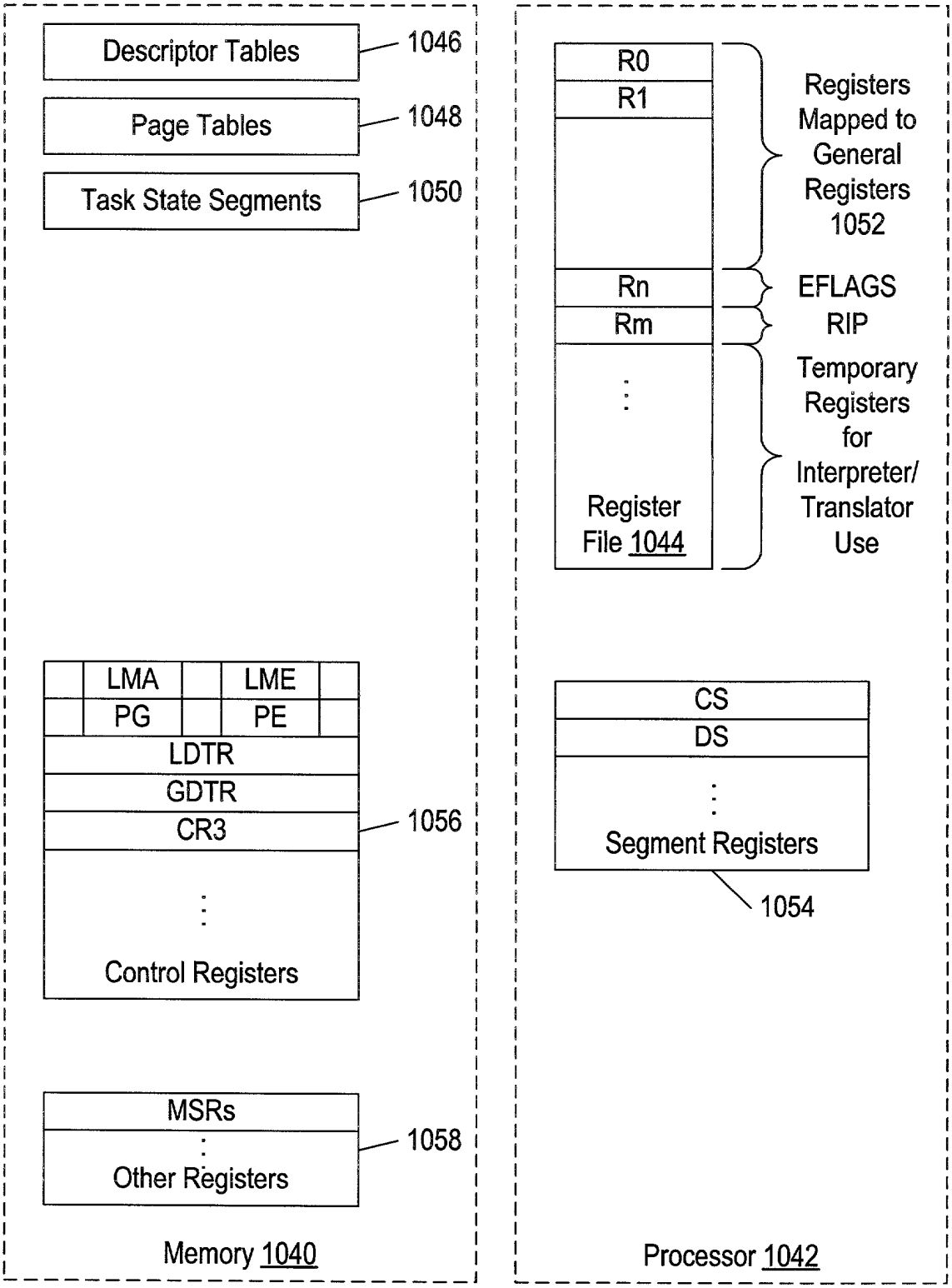

Descriptor Tables
1046
Page Tables
1048
Task State Segments
1050
LMA
LME
PG
PE
LDTR
GDTR
CR3
1056
Control Registers
MSRs
1058
Other Registers
Memory 1040
R0
R1
Registers Mapped to General Registers 1052
Rn
EFLAGS
Rm
RIP
Temporary Registers for Interpreter/ Translator Use
Register File 1044
CS
DS
Segment Registers
1054
Processor 1042

Fig. 14

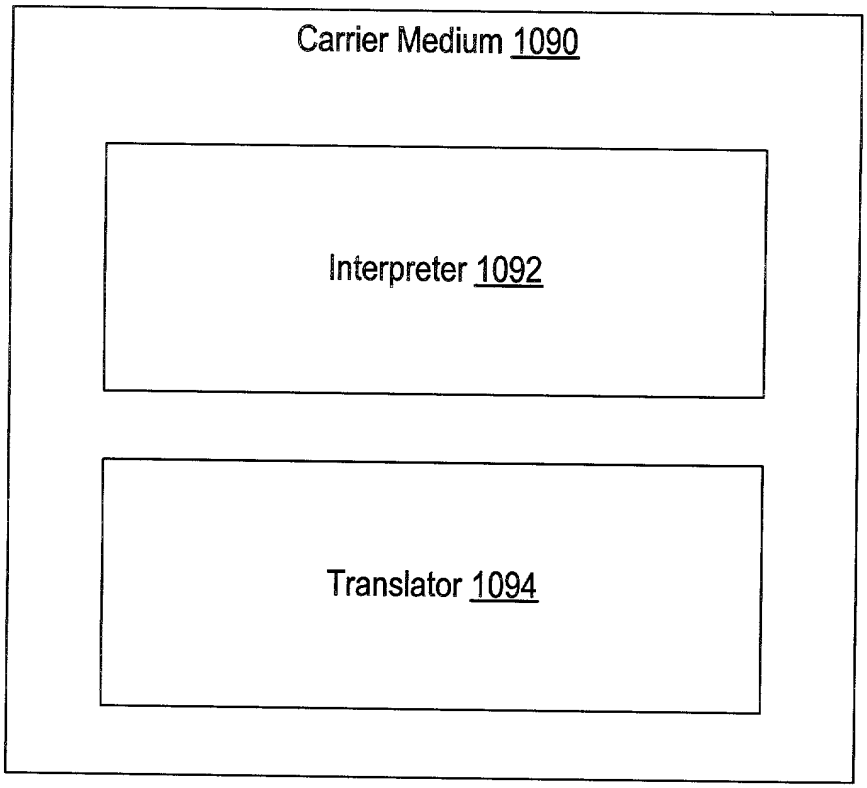


Fig. 15

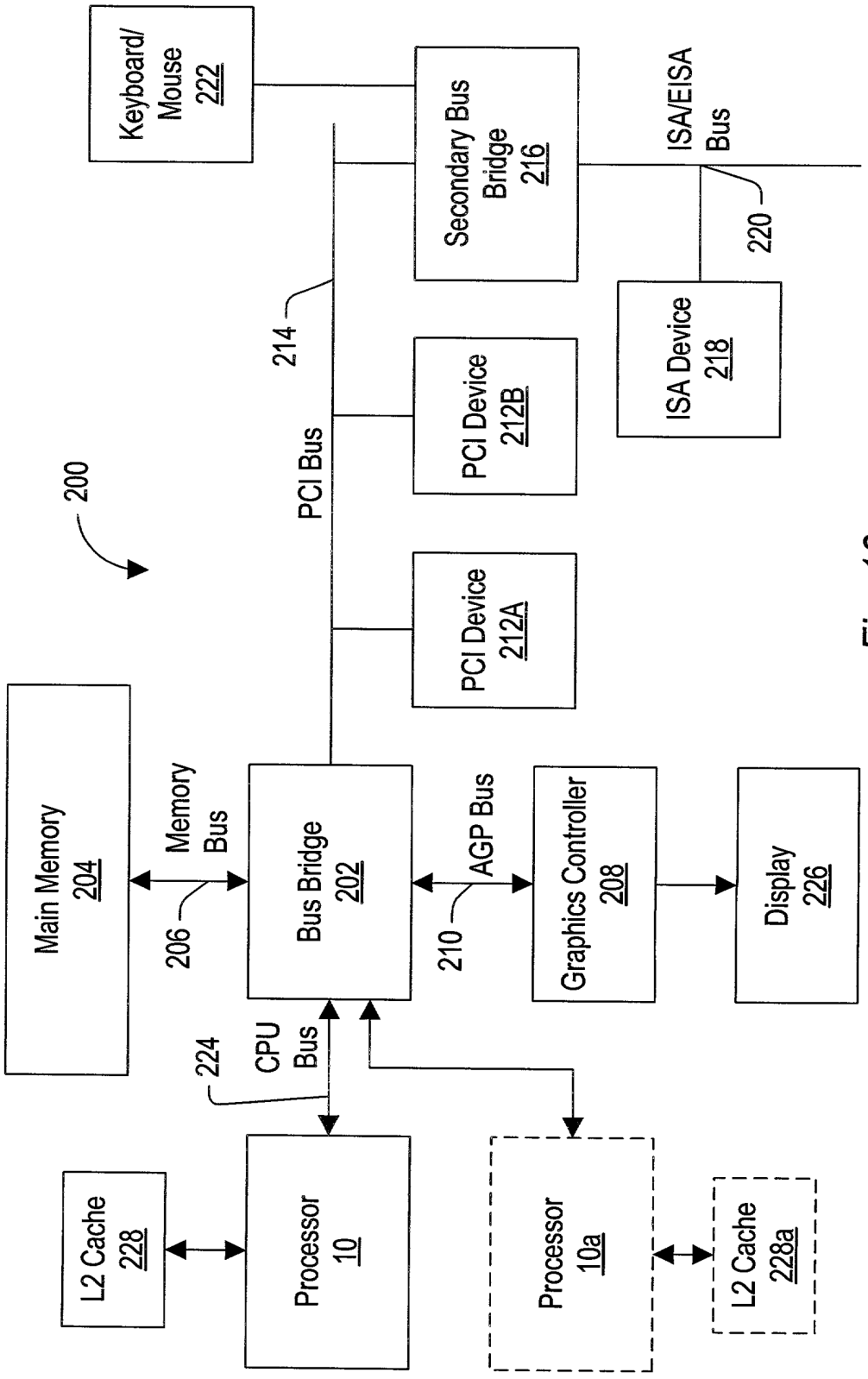

Keyboard/ Mouse 222
Secondary Bus Bridge 216
ISA/EISA Bus
220
214
PCI Bus
PCI Device 212B
ISA Device 218
200
PCI Device 212A
Main Memory 204
Memory Bus
206
Bus Bridge 202
AGP Bus
210
Graphics Controller 208
Display 226
224
CPU Bus
L2 Cache 228
Processor 10
Processor 10a
L2 Cache 228a

Fig. 16

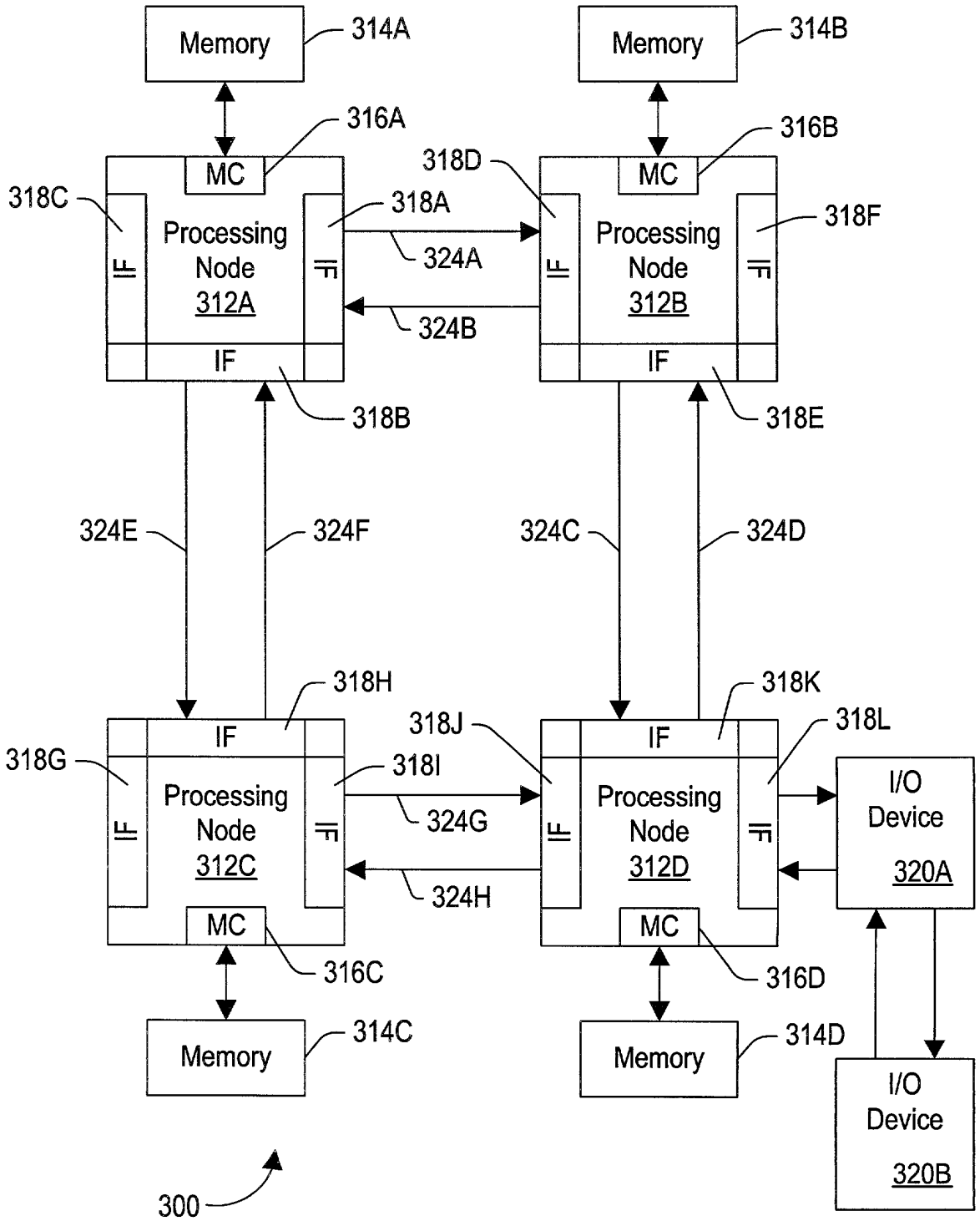

Memory
314A
Memory
314B
316A
316B
MC
MC
318D
318C
318A
318F
IF
Processing Node 312A
IF
IF
Processing Node 312B
IF
324A
324B
IF
IF
318B
318E
324E
324F
324C
324D
318H
318K
318J
318L
IF
IF
318G
318I
IF
Processing Node 312C
IF
IF
Processing Node 312D
IF
I/O Device 320A
324G
324H
MC
MC
316C
316D
Memory
314C
Memory
314D
I/O Device 320B
300

Fig. 17